R16

Code No: 138AQ

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech IV Year II Semester Examinations, July - 2023

ANALOG CMOS IC DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	What are the various models to represent a MOS transistor?	[2]
b)	Draw the small signal model of MOS Transistor.	[3]
c)	What is mean by current sink?	[2]
d)	Draw the circuit diagram of MOS Cascode current mirror.	[3]
e)	What is an active load amplifier?	[2]
f)	What are the advantage of Cascode amplifier? Where it is used?	[3]
g)	Why compensation is needed in op-amp?	[2]
h)	Explain the charge injection error and why it is occur?	[3]
i)	List the important characteristics of a comparator.	[2]
j)	Define propagation time delay in comparator.	[3]

PART – B

(50 Marks)

2.a)	Explain the Large-signal model for the MOS Transistor.	
b)	Explain about the computer simulation models.	[5+5]
	OR	
3.a)	Explain about the CMOS device Modeling.	
b)	With the help of required expressions explain Sub-threshold MOS Model.	[5+5]
4.a)	Discuss about current and voltage references in detail with suitable diagrams.	
b)	What is beta helper? How is it used in current mirrors?	[5+5]
	OR	
5.a)	Draw and explain the circuit diagram of cascade current mirror.	
b)	Write a short notes on current sources with neat circuit diagram.	[5+5]
6.a)	Design a differential amplifier using CMOS transistors and explain its working.	
b)	Discuss the CMOS inverter in detail with the explanation of VTC.	[5+5]
	OR	
7.a)	Design a CMOS current mirror load differential amplifier.	
b)	Explain the slew rate and noise for p-channel differential amplifier with necessary equations.	[5+5]

8. With neat sketch and necessary equations explain the concept of nulling resistor compensation of two stage CMOS Op-Amp. [10]

OR

9. List various compensation techniques of Op-Amps, explain feed forward compensation. [10]

10. Build the circuit model and frequency response of two stage comparator. [10]

OR

11. How to improve the performance of Open loop comparator? Explain. [10]

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